Large-grain polycrystalline silicon films with low intragranular defect density by low-temperature solid-phase crystallization without underlying oxide

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The solid-phase crystallization of an amorphous silicon film to polycrystalline silicon by a low-temperature ($\leqslant$600 °C) furnace anneal has been investigated in a suspended cantilever structure without underlying silicon oxide by transmission electron microscopy and Raman spectroscopy. The grain size of polysilicon increases up to $\sim$3.0 μm and the density of intragranular defects decreases one order of magnitude in the samples without underlying oxide, compared with those with underlying oxide. The main reasons for the high quality of the suspended structures are thought to be due to the lower stress in the films during crystallization and a reduced grain nucleation rate. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1448395]

I. INTRODUCTION

Polysilicon films crystallized from amorphous silicon have been of great interest for active layers in the thin film transistors (TFTs), which are used to drive and switch the image pixels in active matrix liquid crystal displays (AMLCD)[1] and also used in silicon-on-insulator (SOI) technologies for three-dimensional integrated devices.[2] The electrical characteristics of polysilicon TFTs are strongly dependent on the polysilicon microstructure. Grain boundaries and intragranular defects are electrical potential barriers and scattering sites, which decrease the carrier transport mobility and also serve as midgap states to increase the leakage currents. Polysilicon films with larger grain sizes and fewer intragranular defects have been a continual goal.[3–6]

Recent low temperature ($\leqslant$600 °C) solid phase crystallization (SPC) techniques can achieve a grain size as large as 3.0 μm deposited by disilane gas.[3] TFTs made with channel lengths smaller than the grain size still have the mobility only on the order of 100 cm^2/Vs, even though there should be no grain boundaries within the channel. However, the residual intragranular defects reduce the defect-free area of polysilicon film down to 30 nm, and it is thought that they become the limiting factor in device performance.[7] Therefore, reducing the density of intragranular defects becomes very important to improve the electrical performance of TFTs. To date, two methods have been suggested to reduce the density of intragranular defects: high-temperature annealing[7,8] and laser crystallization.[9] Haji *et al.*[7] reported that main intragranular defects in polysilicon films after crystallization at 600 °C are microtwins, that they are not stable above 750 °C, and that they can be eliminated after further high-temperature annealing. However, high-temperature processing cannot be applied to AMLCD TFTs fabricated on glass substrates with a strain point less than 650 °C. Compared with the furnace annealing, laser crystallization has disadvantages of high cost and poor film uniformity. Reducing this intragranular defect density of SPC polysilicon films at a temperature below 650 °C is a motivating factor for this research.

In this work, a free-standing cantilever of amorphous silicon film without underlying silicon dioxide was fabricated. The absence of underlying oxide is found to decrease the intragranular defect density and increase the grain size.

II. EXPERIMENTAL DETAILS

Figure 1 shows the fabrication process of the cantilever structure and its layer structure. Before amorphous silicon (*a*-Si) film deposition, 100-nm-thick silicon nitride was deposited by low-pressure chemical vapor deposition on a $\langle 100 \rangle$ silicon substrate. The purpose of Si_3N_4 here is to alleviate the ''stiction'' problem during the cantilever release process. Two-micrometer-thick silicon dioxide at 250 °C and subsequently amorphous silicon at 150 °C were deposited by plasma-enhanced chemical vapor deposition. During *a*-Si deposition, the flow rate of silane is 50 sccm, pressure stabilizes at 0.5 Torr, and the radio frequency power is $\sim$18

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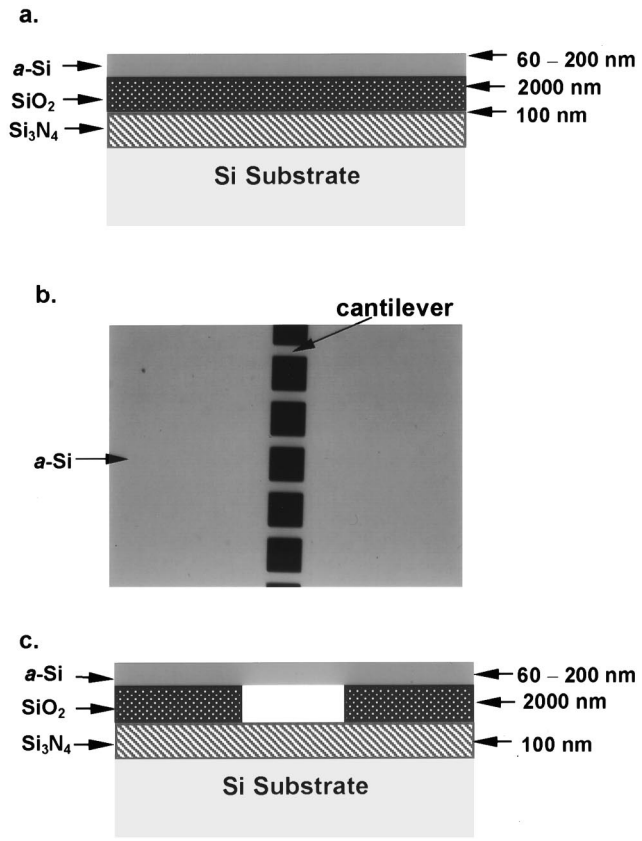

FIG. 1. Fabrication process of amorphous silicon cantilever structure: (a) layer structure; (b) top view before silicon dioxide etching; (c) cross section of cantilever structure after wet etching in buffered oxide etch (10:1).

mW/cm^2. The hydrogen concentration in *a*-Si films is ~17 at. %. The amorphous silicon was then patterned into islands [Fig. 1(b)] by optical lithography and dry etching. Oxide wet etching in buffered oxide etch 10:1 (H_2O:HF) for 30 min was used to release the cantilevers, which have a typical length and width of 20 μm and 10 μm, respectively. Stiction was avoided by rinsing in DI water, soaking in isopropanol, and finally heating on a hot plate at 200 °C for 20 s to evaporate isoproponal. Scanning electron microscopy (SEM) observation [Fig. 2(a)] confirmed that the *a*-Si cantilevers did not collapse onto the substrate. Samples were then annealed at 600 °C for various periods in nitrogen to crystallize amorphous films to polysilicon.[10] SEM again confirmed the suspension of the polysilicon cantilevers [Fig. 2(b)]. The effect of the cantilever was determined by comparing the polysilicon properties on them with that in areas on the same sample when the underlying SiO_2 was not removed (control area).

Transmission electron microscopy (TEM) samples were prepared by a lift-off process. After patterned and etching in a concentrated HF solution, islands with ~2.0 mm diameters were released from the oxidized silicon substrate and were then manually placed onto copper grids for TEM observation. The grain size of polysilicon was calculated by the formula of $d=\sqrt{4A/\pi}$, where A is the area of a grain.

The Raman scattering spectra of polysilicon films were measured at room temperature from 400 cm^{-1} to 600 cm^{-1} wavenumbers, using an argon laser source with a wavelength of 514.5 nm. To prevent further heating and crystallization of silicon films during experiment, the laser power was below 50 mW. The Raman data were fitted to a combination of Lorentzian and Gaussian modes for peak parameters.

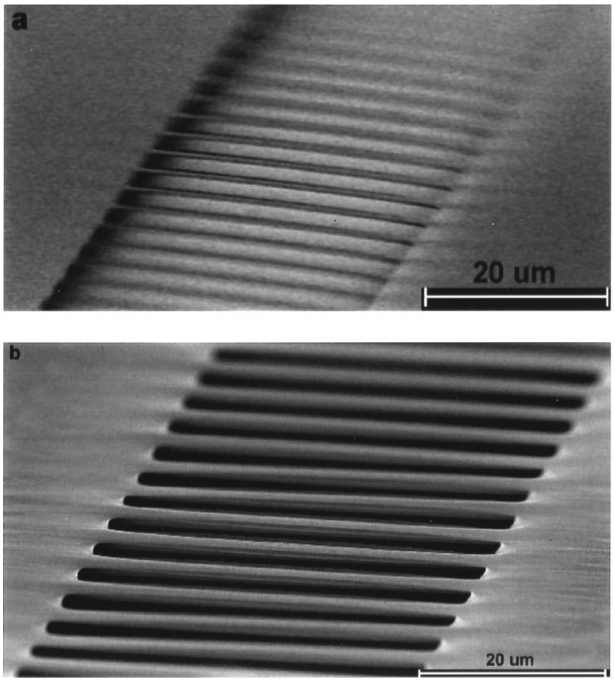

FIG. 2. SEM observations to show the silicon cantilever suspended above the substrate (a) before annealing and (b) after annealing.

III. RESULTS AND DISCUSSION

A. Grain size enhancement

Figure 3 shows TEM observations of fully-crystallized polysilicon grains in (a) control regions with underlying SiO_2 and in (b) cantilever regions without underlying SiO_2, after annealing at 600 °C for 24 h. The inset of (a) is the diffraction pattern of the polysilicon films. The average grain size is ~3.0 μm in (a), 0.6 μm in (b). This indicates that the removal of SiO_2 under the amorphous silicon layer before annealing increases the grain size of polycrystalline silicon.

The solid-phase crystallization of amorphous silicon involves two steps, i.e., nucleation and growth. The increase in grain size can be explained by a decrease in the nucleation rate or an increase in the grain growth rate, both leading to fewer but larger grains. A theoretical analysis by Iverson and Reif[11] gave the final grain size d by

$$d \propto [\nu_g / N]^{1/3},$$

where N is the nucleation rate, and ν_g is the grain growth rate. It has been pointed out that the interface of the precursor amorphous film/substrate (a-Si/SiO_2) is the preferred site for SPC nucleation.[12] A large number of nucleation sites at the interface of a-Si/SiO_2 in the typical SPC films results in small silicon grains due to their impingements during grain growth. Ryu *et al.*[5] claimed that when the nucleation at the interface between the *a*-Si:H and the underlying SiO_2 has been suppressed by adding oxygen to the initially growing *a*-Si, the resulting slower top surface nucleation of amorphous silicon can increase polysilicon grain size from 0.3

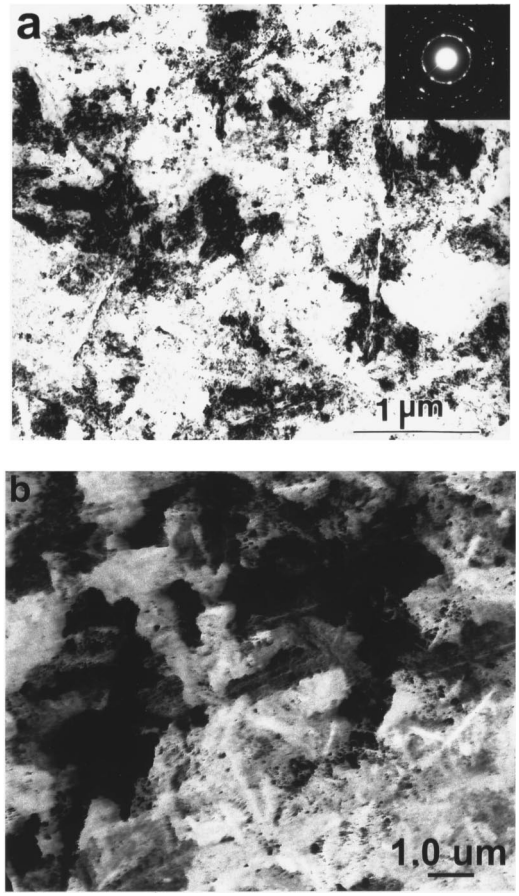

FIG. 3. Plane-view TEM micrographs to show the grain size of fully-crystallized polysilicon films after annealing at 600 °C for 24 h in (a) control region with underlying SiO_2 (grain size ~0.6 μm) and (b) cantilever region without underlying SiO_2 (grain size ~3.0 μm). Inset of (a) is the diffraction pattern of polysilicon films.

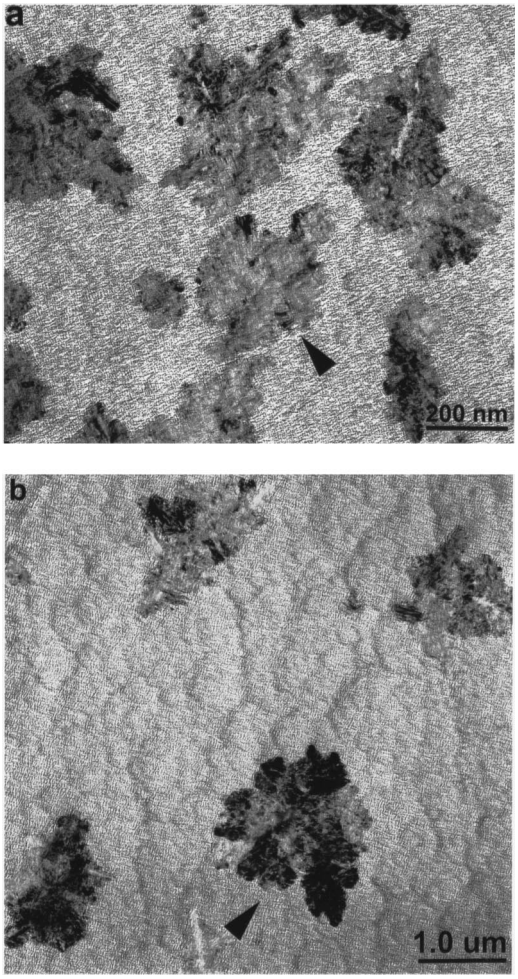

FIG. 4. TEM observations of the grain density and grain size in (a) as-controlled films and (b) suspended films after annealing at 600 °C for 14 h before complete crystallization.

~1 μm to 3~5 μm. Instead of incorporating of oxygen atoms into the initial growing *a*-Si:H, we etched away the underlying SiO_2 to completely remove the interface associated with the nucleation. Figure 4 shows the grain density within *a*-Si: H matrix after heating at 600 °C for 14 h before complete crystallization in (a) the control region and (b) the cantilever region. The grain density in the free-standing films is ~10 times lower than in the control films (~10^8 cm^{-2} versus ~10^7 cm^{-2}). This smaller nucleation rate N in the cantilever sample is one reason leading to the final larger grains.

Besides the difference of grain density before full crystallization, the grain size in the control film before merging of the grains is smaller than that in the cantilever film. An average grain in the control film [pointed to by an arrow in Fig. 4(a)] has a size ~0.4 μm, while that in the cantilever films [Fig. 4(b)] is ~1.0μm. Therefore, the growth velocity of polysilicon grains can be increased by the removal of the underlying SiO_2 before crystallization. Thus the larger grain size in the fully crystallized suspended versus control films as shown in Fig. 3 is attributed not only to the lower nucleation density N, but also to the higher growth rate ν_g.

During the growth stage of SPC, growth rate ν_g has been expressed as[11]

$$\nu_g \propto \exp[-(E_d+\Delta G/2)/kT],$$

where E_d is the activation energy of silicon atom self-diffusion, and ΔG is the net free energy during SPC, which has been expressed as

$$\Delta G = -V\Delta G_v + A\gamma + V\Delta G_s,$$

where ΔG_v is Gibbs-free-energy difference between *a*-Si and polysilicon per unit volume V, γ is the interface energy per unit surface area A, and ΔG_s is strain energy per unit volume V related to the phase transition. Stress can accumulate during SPC due to volume contraction on *a*-Si to poly-Si phase transition, or due to inability of silicon atoms to freely rearrange near the *a*-Si/SiO_2 interface due to the bonding of *a*-Si atoms to the oxide. The strain energy ΔG_s results from this stress during SPC. The difference of the final stress in the SPC films was measured by Raman scattering, which detects the energy of optical phonons that interact with a probe photon beam. The shift in phonon energy (Raman shift) depends on the stress in the material, with biaxial tension leading to a smaller Raman shift.[13,14] Fig. 5(a) shows the Raman spectra of 200-nm-thick polysilicon films crystallized with and without underlying SiO_2 and of ⟨100⟩-bulk silicon. The Raman peak for both free-standing cantilever

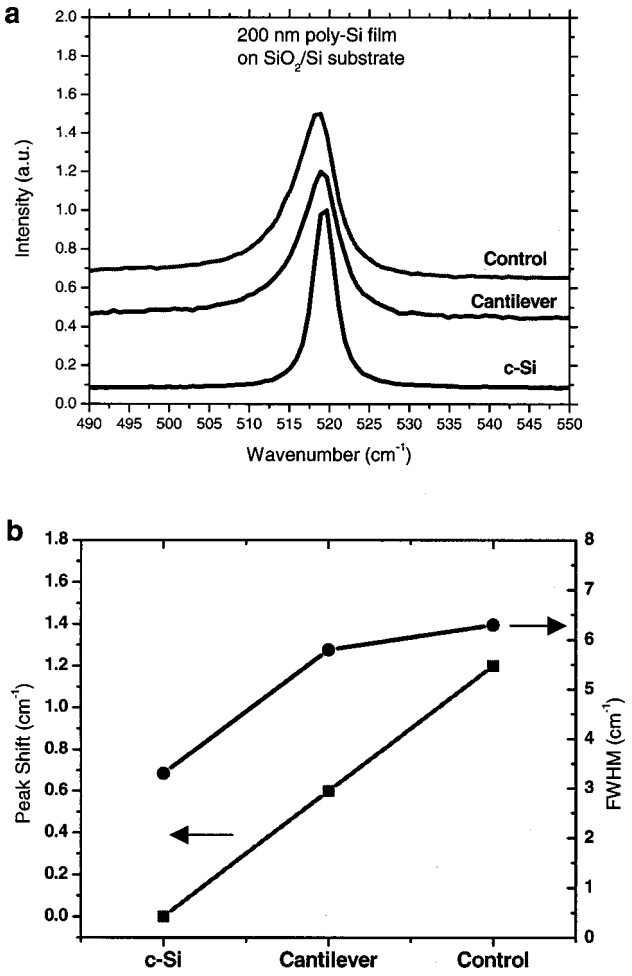

FIG. 5. (a) Raman spectra and (b) peak-shift and FWHM of polysilicon films in the control region and cantilever region, and of ⟨100⟩-oriented single-crystalline silicon substrate.

films and the films on oxide are at smaller wavenumbers than that in the single-crystal silicon (519.5 cm^{-1}), confirming tensile stress as would be expected from a volume contraction. By the curve fitting, the Raman shift and the full width at half magnitude (FWHM) of the spectra are plotted in Fig. 5(b). The Raman scattering energy is lower in the cantilever films vs. the control SPC films, indicating the higher residual stress existing in the as-controlled polysilicon films. According to the following equation:[14]

$$\sigma(\mathrm{MPa}) = -250\Delta\omega(\mathrm{cm}^{-1}),$$

where σ is the in-plane stress and $\Delta\omega = \omega_s - \omega_0$, the tensile stress in the control polysilicon film is ~300 MPa, whereas the stress in the cantilever film is only ~150 MPa. This reduction of tensile stress in the cantilever structure could result either because the cantilever film can laterally relax in the direction perpendicular to the cantilever length to relieve tensile stress due to the volume contraction, or because removal of the underlying SiO_2 leads to a free motion of silicon atoms at the bottom surface of silicon films. Less stress in the cantilever films should result in a lower strain energy ΔG_s, and thus increase the driving force for the grain growth and grain growth velocity.

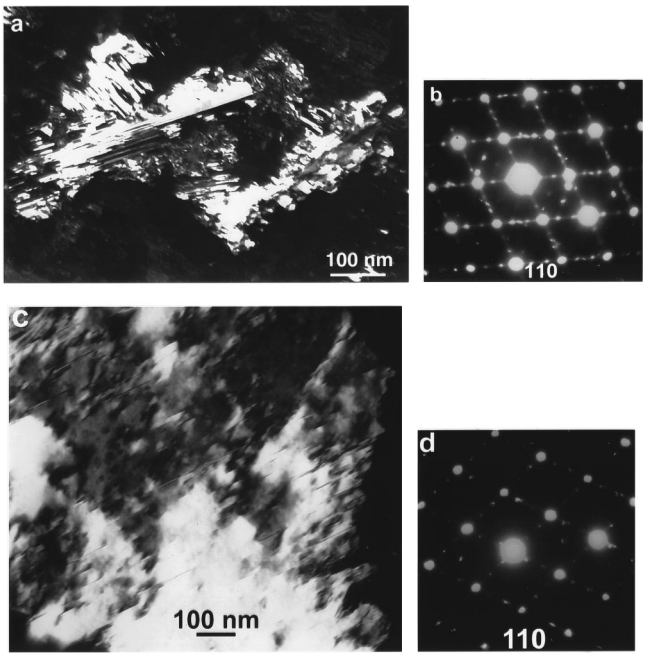

FIG. 6. Dark-field TEM micrographs and their selected area (~300 nm in diameter) diffraction pattern in the control sample (a and b) and in the cantilever sample (c and d). Streaks and extra spots in the SADP of (b) and (d) with ⟨110⟩ crystallographic orientations parallel to the electron beam result from the intragranular defects.

B. Reduced intragranular defect density

The main defects within polysilicon grains crystallized by furnace annealing are microtwins and dislocations.[7,15] Microtwins in polysilicon grains occur on {111} planes.[7,16] Therefore, observation under ⟨110⟩ orientation will make the microtwins clearly visible in TEM, where the intersection line between the twin plane {111} and the surface plane {110} denotes the microtwin. The difference in intragranular defect density between the control and the cantilever structures was measured in 60-nm-thick samples annealed at 600 °C for 20 h. Figure 6 shows the dark-field images of silicon grains and their selected area diffraction patterns (SADP) (from regions ~300 nm in diameter) in (a and b) control regions and (c and d) cantilever regions. The observed grain orientations are ⟨110⟩ (indexed from the diffraction patterns) in both cases. The high density of microtwins in the control film grains is very obvious, giving rise to the extra spots and streaks in its diffraction pattern. Although the polysilicon grains in the cantilever film [Fig. 6(c)] are not free of defects, the density of intragranular defects is much lower, and therefore, there are fewer extra spots and streaks in the diffraction pattern of Fig. 6(d) than in Fig. 6(b). In the control sample [Fig. 6(a)], the defect-free area between defects observable under high resolution is ~25 nm in diameter on the average, which is consistent with the previous work on polysilicon from SPC at 600 °C.[7] However, the defect-free area in the cantilever films reaches ~100 nm. Defining a defect density as the inverse of the defect-free area, the intragranular defect density in the cantilever samples is almost one order of magnitude lower than that in the control samples (~10^{10} cm^{-2} versus ~10^{11} cm^{-2}).

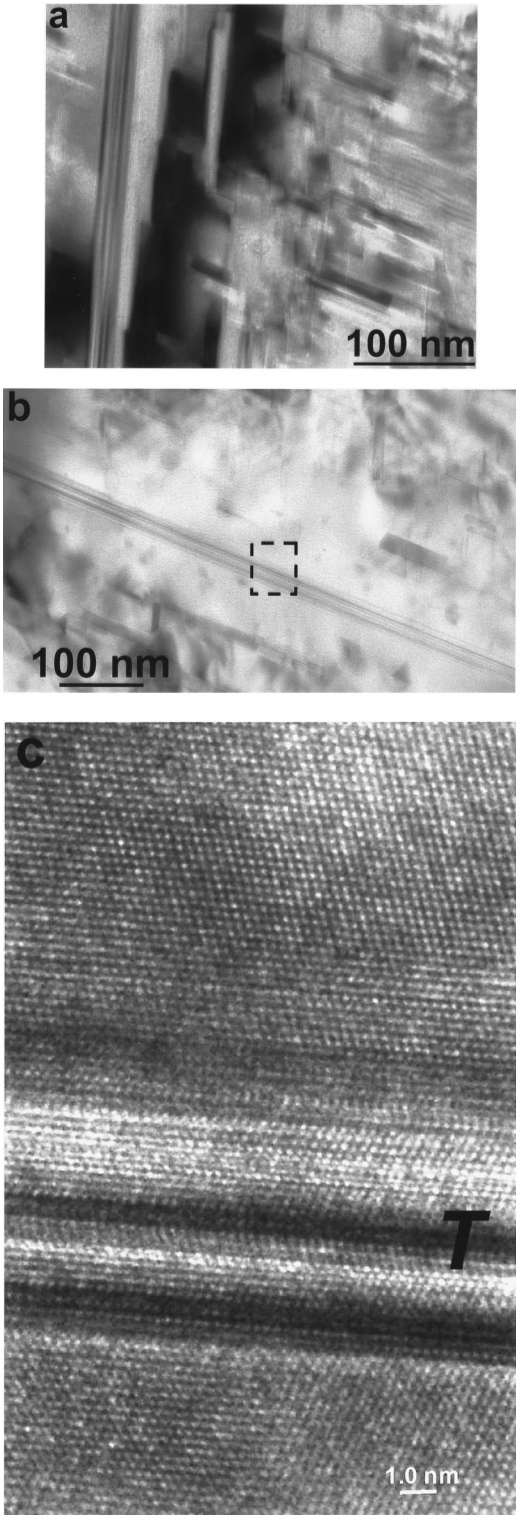

FIG. 7. High-magnification bright-field TEM observations on polysilicon grains in (a) the control region and (b) the cantilever region. The electron beam was parallel to ⟨110⟩ crystallographic orientation of the silicon grains. (c) High-resolution TEM image of polysilicon films in the cantilever area marked by the dashed-lines in (b). Very regular lattice fringes with d_{111} spacing are very evident. Coherent microtwins are denoted by a letter "*T*."

High-magnification TEM observations on the intragranular defect density are shown in Fig. 7 with the electron-beam aligned to the ⟨110⟩ orientation of the grain. The microtwin lines are clearly visible, and the defect-free area in the control region [Fig. 7(a)] is much smaller than that in the cantilever region [Fig. 7(b)]. High-resolution TEM micrograph on very small area marked in Fig. 7(b) shows the atomic arrangements around the microtwins, denoted by a letter "T." On both sides of the microtwins, periodic (111) planes are clearly seen.

It is well known that small crystallites and high defect densities in polysilicon films cause asymmetry and broadening of the Raman spectrum due to phonon scattering from the microcrystalline boundaries.[17–19] The crystallite size for this effect can be defined by both grain boundaries as well as intragranular defects.[20] The defect scattering destroys the lattice translational symmetry and relaxes the momentum conservation rule governing the creation and decay of phonons, so that smaller size of the microcrystallites increases the Raman FWHM.[17–21] In Fig. 5(b), the values of FWHM of Raman spectra in various regions are: cantilever polysilicon region, 5.8 cm^{-1}; control polysilicon region, 6.3 cm^{-1}; and single-crystalline silicon substrate, 3.3 cm^{-1}. This narrower peak in the cantilever region suggests a lower density of intragranular defects compared with that in the control region in qualitative agreement with our TEM observations.

The reason for reduced intragranular defect density is now discussed. As mentioned earlier, SPC of *a*-Si to polysilicon requires the rearrangement of silicon atoms at the interface of a-Si/SiO_2, and also accompanies a volume contraction, both leading to tensile stress in the silicon films. To relieve this stress, crystalline defects (microtwins, dislocations, etc.) develop during the nucleation stage[22] and growth stage.[16] This stress is largest at the a-Si/SiO_2 interface as the silicon atoms in the *a*-Si are strongly bound to the surface atoms of the underlying SiO_2 layer after deposition.[23] As the nucleation predominantly occurs at the interface, defect density is quite high in the typical SPC films. However, Morimoto *et al.*[4] have demonstrated the formation of nearly defect-free crystalline silicon film by removing the underlying SiO_2 before annealing during lateral solid-phase epitaxy seeded from a [100] silicon substrate. In this paper, removing the SiO_2 underlying the *a*-Si suppressed a-Si/SiO_2 interface nucleation, although the dominant nucleation is still expected to be at the top or bottom free surfaces of *a*-Si. Since the silicon atoms at the surface are only loosely bound to the native SiO_2 layer on a cantilever, the stress generated upon nucleation can be easily relieved, so fewer defects could be expected. During the subsequent lateral growth of grains in the cantilever, the easier rearrangement of silicon atoms at the surfaces and the relaxation of stress from volume contraction in the silicon films during SPC also result in fewer intragranular defects being created.

IV. CONCLUSIONS

By fabricating a free-standing silicon film without underlying silicon dioxide, the quality of polysilicon films resulting from unseeded SPC of amorphous silicon at 600 °C has been improved. The nucleation density has been decreased and the grain growth rate increased, leading to an average grain size up to 3.0 μm, 50 times larger than that in the films with underlying oxide. Furthermore, the intragranular defect

density has been reduced one order magnitude from $\sim 10^{11}$ cm^{-2} to $\sim 10^{10}$ cm^{-2}. These improved qualities are thought to result from the lower stress in the films crystallized without underlying oxide.

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